LIGHTING SYSTEM AND METHOD FOR A GRAPHICS PROCESSOR

IN THE SPECIFICATION

Please delete lines 7-24 on page 1, and insert therefor: (See Appendix A for redlined copy)

The present application is a continuation of an application filed 12/06/99 under serial number 09/454,524. The present application is further related to applications entitled "Method, Apparatus and Article of Manufacture for Area Rasterization using Sense Points" which was filed on December 06, 1999 under serial number 09/455,305, and attorney docket number NVIDP005, "Method, Apparatus and Article of Manufacture for Boustrophedonic Rasterization" which was filed on December 06, 1999 under serial number 09/454,505, and attorney docket number NVIDP006, "Method, Apparatus and Article of Manufacture for Clip-less Rasterization using Line Equation-based Traversal" which was filed on December 06, 1999 under serial number 09/455,728, and attorney docket number NVIDP007, "Method, Apparatus and Article of Manufacture for Transform, Lighting and Rasterization on a Single Semiconductor Platform" which was filed on December 06, 1999 under serial number 09/454,516, and attorney docket number NVIDP008, "Method, Apparatus and Article of Manufacture for a Vertex Attribute Buffer in a Graphics Processor" which was filed on December 06, 1999 under serial number 09/454,525, and attorney docket number NVIDP009, "Method, Apparatus and Article of Manufacture for a Transform Module in a Graphics Processor" which was filed on December 06, 1999 under serial number 09/456,102, and attorney docket number NVIDP010, and "Method, Apparatus and Article of Manufacture for a Sequencer in a Transform/Lighting Module Capable of Processing Multiple Independent Execution Threads" which was filed on December 06, 1999 under serial number 09/456,104, and attorney docket number NVIDP012 which were filed concurrently herewith, and which are all incorporated herein by reference in their entirety.

On page 5, please delete lines 7-15, and insert therefor: (See Appendix A for redlined copy)

Figure **1** illustrates the prior art;

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Figure **1A** is a flow diagram illustrating the various components of one embodiment of the present invention implemented on a single semiconductor platform;

On page 11, please delete the first paragraph and insert therefore: (See Appendix A for redlined copy)

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Figure **1** illustrates the prior art. Figures **1A-32C** show a graphics pipeline system of the present invention.

On page 11, please delete the second paragraph and insert therefore: (See Appendix A for redlined copy)

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Figure **1A** is a flow diagram illustrating the various components of one embodiment of the present invention. As shown, the present invention is divided into four main modules including a vertex attribute buffer (VAB) **50**, a transform module **52**, a lighting module **54**, and a rasterization module **56** with a set-up module **57**. In one embodiment, each of the foregoing modules is situated on a single semiconductor platform in a manner that will be described hereinafter in greater detail. In the present description, the single semiconductor platform may refer to a sole unitary semiconductor-based integrated circuit or chip.